

## BEN GERDEMANN

http://www.ibeni.net ✉ resume@ibeni.net  
(41) 9960-6789 ✉ Curitiba, Brazil

A Computer Engineer with experience in software programming and IT administration searching for a challenging position in software development or IT administration.

### SUMMARY

- Graduated from Rice University (Houston, Texas) with a degree in Computer Engineering
- Worked for six years at AMD (Austin, Texas) starting in the International Business Marketing Group managing the relationship with the sales offices in Japan and Korea, then became a Design Engineer implementing next-generation CPUs and finally a Senior Verification Design Engineer overseeing the simulation infrastructure of the data center.
- Studied for one year at Instituto Superior Técnico (Lisbon, Portugal) where I researched using custom-hardware to improve the performance of hardware simulation
- Developed and maintained large software projects including a compiler for custom processors developed from scratch in C++ and an "system model" written in C and used to test the functionality of a complete microprocessor in simulation
- Developed and supported a complete hardware verification environment in Perl including version control, storing results in a database, executing simulations on a bank of remote machines and randomizing the microprocessor simulations
- Hands-on experience administrating more than five-thousand RedHat machines as part of a LSF cluster
- Lead international teams working in Japan and India

### TECHNICAL EXPERTISE

**Programming languages:** C, C++ (including STL and Boost libraries), Java, Lisp, Perl, Python and shell programming

**Programming tools:** CVS, Subversion, Makefile, Distributed Make, LSF

**Programming concepts:** Object-oriented programming, UML diagrams, refactoring, design patterns, unit testing (JUnit)

**Databases:** SQL queries (MySQL), database design and normalization

**Web:** HTML design, PHP

**Operating Systems:** RedHat Enterprise, CentOS, Ubuntu, Windows XP

**EDA languages and tools:** Verilog including PLI, Synopsis VCS, Verplex (Cadence) Logic Equivalence Checker (LEC) and BlackTie, Novas Debussy, Pathfinder

### LANGUAGE SKILLS

**English:** Native speaker

**Japanese:** Advanced level

**Portuguese:** Advanced level

2007-2008

**Instituto Superior Técnico, Lisbon, Portugal**

*Ph.D. Student, Department of Information Systems and Computer Engineering, Grades: 17/20*

- Research interests in reconfigurable computing and verification of multi-core processors using hardware emulation and custom processor techniques
- Developed a prototype compiler using C++ to compile hardware designs into a custom VLIW architecture

#### *Presentations*

- "Accelerating Functional Verification of Microprocessors," *ANCORA-I Workshop*, December 6, 2007, Instituto Superior Técnico, Lisbon.

#### *Papers*

- "Reconfiguring the future of computing," in *Tecnológica* the IT magazine of Instituto Superior Técnico (to appear).
- "Accelerating functional verification of multi-core processors using a VLIW application-specific instruction-set processor (ASIP) for virtual simulation" to be presented as part of the Advanced Topics class (in progress).

#### *Courses*

- Object-Oriented Programming, Databases, Analysis and Synthesis of Algorithms, Artificial Intelligence

2006-2007

**University of Lisbon, Lisbon, Portugal**

*Portuguese Language Course for Foreigners*

Completed Intermediate Level Class

2001-2006

**Advanced Micro Devices, Austin, Texas**

*Senior Verification Design Engineer, 2004 – 2006*

- Worked on “Barcelona” four core design
- Managed, developed and supported in-house and external tools used to compile, simulate and verify the functional RTL design
- Supported “system model” code written in C allowing test patterns to trigger system events
- Managed and debugged regressions of the design over a cluster of ~5,000 machines, including selecting appropriate test patterns, random exercisers and viewpoints of the design while managing computer resources efficiently
- Defined and implemented the infrastructure to run gate simulations comparing the functional RTL and physical implementation
- Defined and implemented a brand new infrastructure for handling forked designs using revision control that seamlessly supported using both shared and unique IP for each design
- Ported the entire design and infrastructure to compile and execute in 64-bits
- Supported a tool for randomizing all possible aspects of the design, updating for new constraints or registers and reviewed randomization coverage with the team
- Mentored three other engineers

*Design Engineer II, 2002 – 2004*

- Worked on Athlon, Opteron and other next generation CPU designs
- Used schematic capture tools to turn functional RTL designs into physical schematics, providing feedback to the designer about optimizations
- Used Chrysalis and Verplex formal verification tools to prove that the physical design matched the functional one and did not violate any electrical properties
- Created a hand placement for the standard cells and worked to meet the project's frequency goal while balancing the design trade-offs of power and area, by optimizing the design placement, buffering, logic and route
- Helped to develop an automated next-generation verification flow, reducing the time for each engineer to verify their block and preventing verification escapes
- Co-simulated the physical and functional design together in a gate simulation to verify that the design would function when coming out of reset

*Product Marketing Engineer, 2001 – 2002*

- Prepared and presented updated forecasts and sales goals for the “North Asia” sales region
- Worked in a team to reach a quarterly sales goal of 800k units shipped
- Consulted with the Japan and Korea sales offices for order scheduling, product sampling and pricing requests
- Acted as a liaison between the regional sales office and engineering headquarters regarding the customer's product and schedule requirements
- Developed software to automatically generate reports that were previously done by hand, improving their accuracy and timeliness

*University Campus Team Member, 2001-2006*

- Helped organize and attended campus recruiting events at Carnegie Mellon University and Rice University
- Judged final student projects of VLSI class at Carnegie Mellon

2000

**National Instruments, Tokyo, Japan**

*Application Engineer Intern*

- Provided e-mail technical support to Japanese customers in Japanese for all NI software and hardware product lines
- Attended a trade show and met with customers on site

1998-1999

**Kyushu University, Fukuoka, Japan**

*Japan in Today's World* exchange program

Studied Japanese language, history and culture, Grades: 3.79/4.00

1998

**Compaq Computer, Houston, Texas**

*Software Test Intern*

1996-2000

**Rice University, Houston, Texas**

B.S. in *Computer Engineering*, B.A. in *Asian Studies*

Classes in *Digital Logic Design, VLSI Design, Digital Circuits and Computer Systems Architecture*, Grades: 3.61/4.00