Accelerating Functional Verification of Multiprocessors

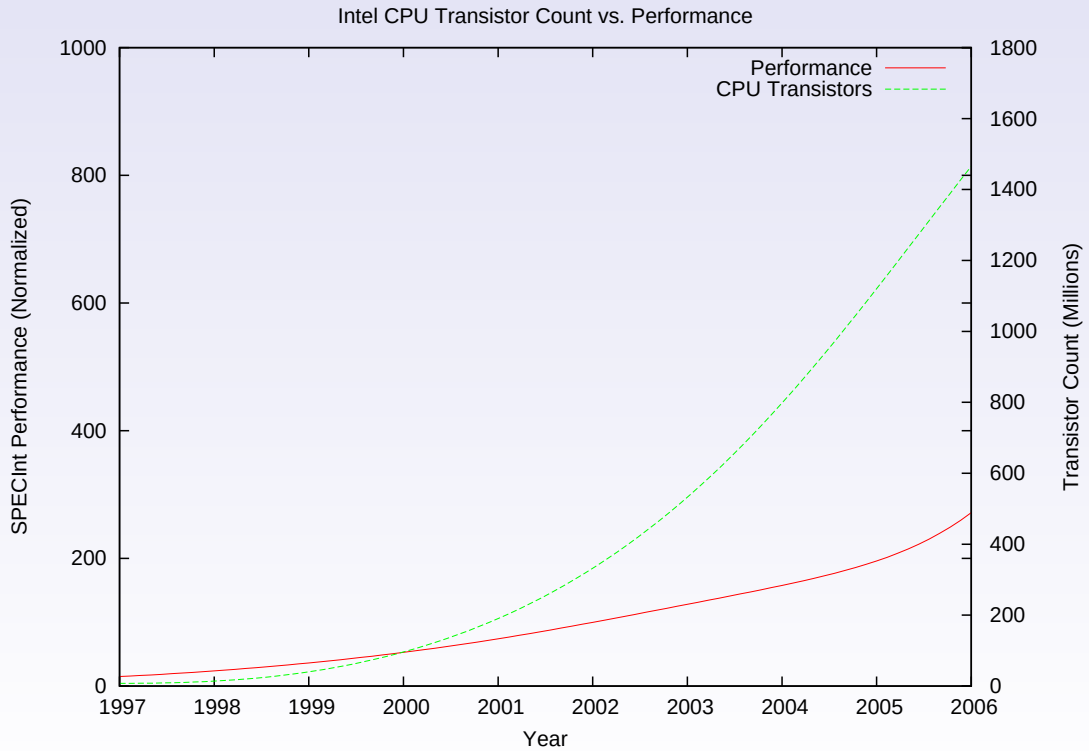
Ben Gerdemann

INESC-ID/Instituto Superior Técnico

June 2008

Background

- Industry estimates are that 50-70% of engineering time spent on a typical microprocessor design is in verification
- The majority of verification effort is focused on functional simulation (test-patterns)
- The performance of functional simulation in software has not scaled with the increasing size of multi-core designs

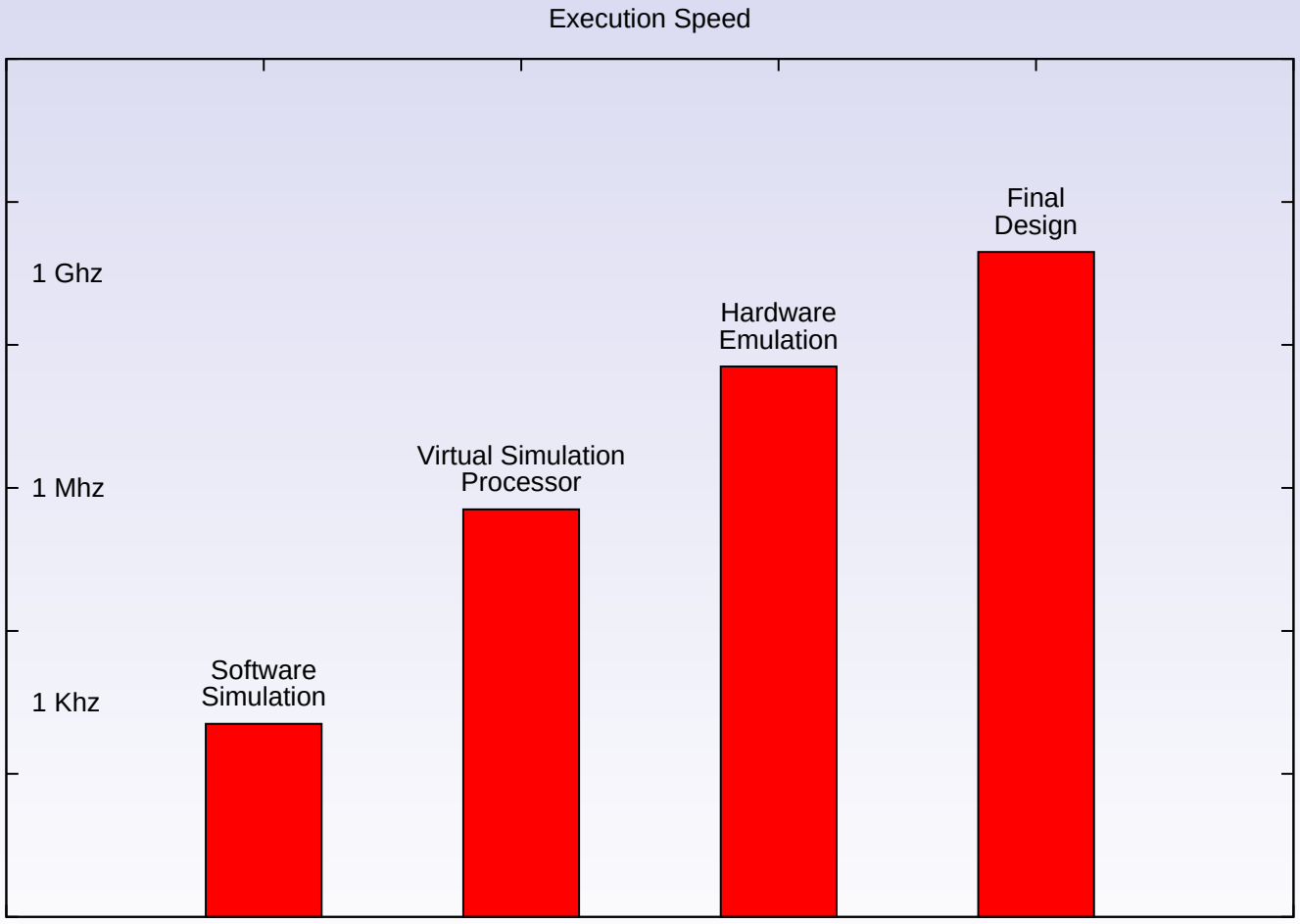


The Problem

Verification times for modern multi-core microprocessors have reached an unacceptable level and have become a major bottleneck to tapeout.

Functional Simulation Options

- There are several ways to functionally simulate a hardware design



Software Simulation

- Hardware description is compiled to a software executable
- Most common and flexible solution
- Any type of design regardless of size or synthesizability can be simulated without modification
- Debugging easily done in software
- Performance of large designs is poor

Hardware Emulation

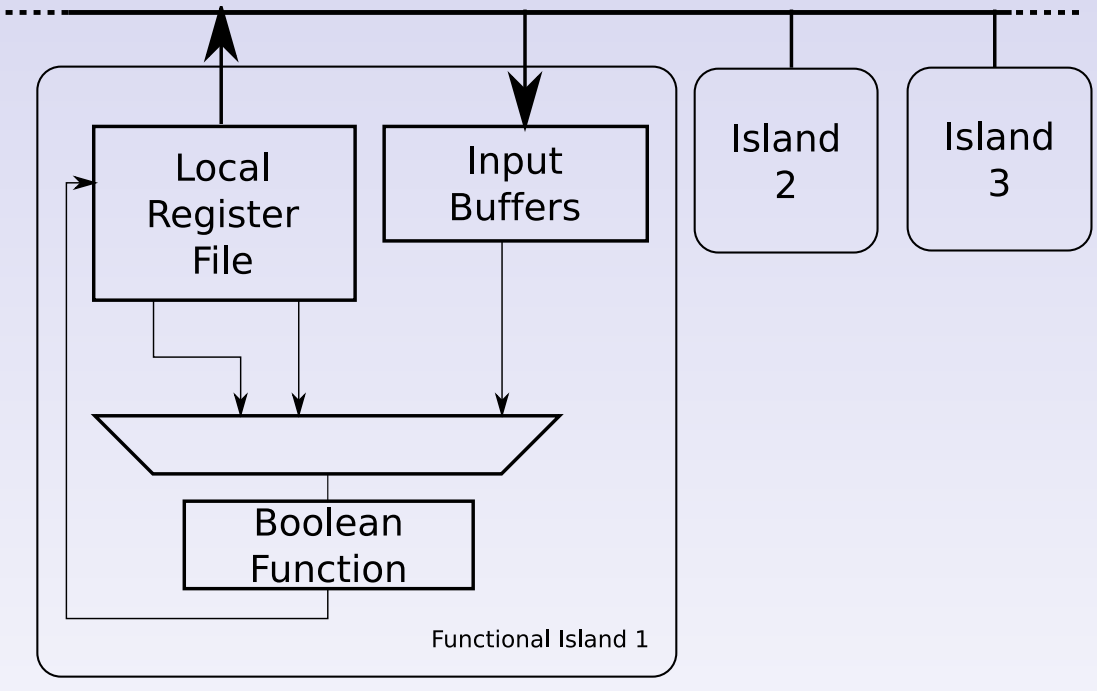
- Design is syntehsized and executed on real hardware
- Typically the emulated design is interfaced with a test-bench in software
- High performance, but places many restrictions on the design
  - Must be synthesizable
  - Timing is restricted
  - May require partitioning to fit on hardware device
- Debugging is difficult
- Often requires remodeling portions of the design (esp. memories and caches) to be feasible
- Typically only deployed at the end of a project, when the design is most static

Virtual Simulation using VLIW on ASIP

Our Solution:

- Compile design into VLIW to be executed on an application specific instruction set processor (ASIP).
- Typical data-flow graph for a hardware design is massively parallel
- Operations are simple boolean functions or register loads and stores
- Use a distributed register-file architecture to support a large number of functional units
- Estimated performance speedup of ~1,000x over software

ASIP Microarchitecture



Project Status

- Prototype compiler
  - Reads hardware design and builds DFG
  - Instructions customized based on number of functional units, size of register file and inter-island bus width
- Hardware design
  - Proof of concept architecture built in Verilog
  - Synthesized onto an FPGA to measure area and timing
  - Has not been simulated yet